**REMARKS**

Applicant would like to thank the Examiner for the thorough examination of the present application, and for the courtesies extended during the telephone interview on November 19, 2003.

Independent Claims 23, 32 and 36 have been amended to more clearly define the present invention over the cited prior art references. As discussed in the interview, the independent claims have been amended to better highlight the fact that "the sidewalls of the outwardly extending dielectric layer are aligned with the sidewalls of the trench." The claim amendments and arguments supporting patentability of the claims are presented in detail below.

**I. Independent Claim 23 Is Patentable**

The Examiner rejected independent Claim 23 over the Applicant's prior art FIGS. 1 and 3a-3b.

Amended independent Claim 23 is directed to a MOSFET comprising a semiconductor layer having a trench therein, a gate dielectric layer lining the trench, and a gate conducting layer in a lower portion of the trench. A dielectric layer is in an upper portion of the trench. The MOSFET further includes source regions adjacent the dielectric layer, and source/body contact regions laterally spaced apart from the gate conducting layer and non-interruptibly contacting the source regions. Independent Claim 23 has been amended to recite that the dielectric layer extends outwardly from the semiconductor layer, the source regions and the source/body contact regions, and the outwardly extending dielectric layer has sidewalls aligned with sidewalls of the trench.

The MOSFET is advantageously formed with the upper portion of the dielectric layer in the trench extending outwardly from the semiconductor layer, the source regions, and the source/body contact regions wherein sidewalls of the outwardly extending dielectric layer are aligned with sidewalls of the trench. This feature of the present invention advantageously allows spacers to be formed laterally adjacent the outwardly extending dielectric layer, which are then used as self-aligned masks for implanting dopants into the semiconductor layer.

In addition, the on-resistance is reduced since each MOSFET includes a source/body contact region that is laterally spaced apart from the gate conducting layer and non-interruptibly contacts the source regions. The source/body contact regions thus provide an efficient short between the source and body regions of the MOSFET. As a result, device ruggedness is increased.

Referring now more particularly to the Applicant's prior art FIGS. 1 and 3a-3b, FIG. 1 illustrates a surface dielectric layer **20** that overlays a portion of the N+ source regions **26**. As clearly illustrated in FIG. 1, the sidewalls of the dielectric layer **20** extend well past the sidewalls of the trench.

In FIGS. 3a-3b, the Examiner has taken the position that the dielectric layer **20** extends outwardly from the semiconductor layer **16**. Independent Claim 23 has been amended to recite that the dielectric layer also extends outwardly from the source regions and the source/body contact regions. In FIGS. 3a-3b, an upper surface of the source regions **26** and an upper surface of the source/body contact regions **18** are

substantially even with an upper surface of the dielectric layer **20**.

The Applicant's prior art figures thus fail to teach or suggest that the dielectric layer extends outwardly from the source regions and the source/body contact regions, as in amended independent Claim 23 in which the sidewalls of the outwardly extending dielectric layer has sidewalls aligned with the sidewalls of the trench. Accordingly, it is submitted that independent Claim 23 is patentable over the Applicant's prior art FIGS. 1 and 3a-3b.

**II. Independent Claims 32 And 36 Are Patentable**

The Examiner rejected independent Claims 32 and 36 over the Applicant's prior art FIGS. 1 and 3a-3b in view of the Gilbert et al. patent.

Amended independent Claim 32, for example, is directed to a MOSFET comprising a semiconductor layer having a trench therein, a gate dielectric layer lining the trench, and a gate conducting layer in a lower portion of the trench. A dielectric layer is in an upper portion of the trench. The MOSFET further includes source regions adjacent the dielectric layer, and source/body contact regions laterally spaced apart from the gate conducting layer and non-interruptibly contacting the source regions. Independent Claim 32 has been amended to recite that the dielectric layer extends outwardly from the semiconductor layer, the source regions and the source/body contact regions, and the outwardly extending dielectric layer has sidewalls aligned with sidewalls of the trench. A source electrode is on the source regions and on the dielectric layer, and at least one conductive via is

between the source electrode and the source/body contact regions.

As noted above, the MOSFET is advantageously formed with the upper portion of the dielectric layer in the trench extending outwardly from the semiconductor layer, the source regions, and the source/body contact regions wherein the sidewalls thereof are aligned with the sidewalls of the trench. This feature of the claimed invention advantageously allows spacers to be formed laterally adjacent the outwardly extending dielectric layer, which are then used as self-aligned masks for implanting dopants into the semiconductor layer.

Referring again to the Applicant's prior art FIGS. 1 and 3a-3b, FIG. 1 illustrates a surface dielectric layer **20** that overlays a portion of the N+ source regions **26**. As clearly illustrated in FIG. 1, the sidewalls of the dielectric layer **20** extend well past the sidewalls of the trench.

In FIGS. 3a-3b, the Examiner has taken the position that the dielectric layer **20** extends outwardly from the semiconductor layer **16**. Independent Claim 32 has been amended to recite that the dielectric layer also extends outwardly from the source regions and the source/body contact regions. In FIGS. 3a-3b, an upper surface of the source regions **26** and an upper surface of the source/body contact regions **18** are substantially even with an upper surface of the dielectric layer **20**.

The Examiner cited the Gilbert et al. patent as disclosing at least one conductive via between the source electrode and the source/body contact regions. However,

Gilbert et al. fails to provide the noted deficiencies with respect to FIGS. 1 and 3a-3b.

The Applicant's prior art figures and the Gilbert et al. patent thus fail to teach or suggest that the dielectric layer extends outwardly from the source regions and the source/body contact regions, as in amended independent Claim 32. Accordingly, it is submitted that independent Claim 32 is patentable over the Applicant's prior art FIGS. 1 and 3a-3b.

Amended independent Claim 36 is similar to independent Claim 32. Accordingly, it is submitted that independent Claim 36 is patentable over the Applicant's prior art FIGS. 1 and 3a-3b in view of the Gilbert et al. patent. In view of the patentability of independent Claims 23, 32 and 36, it is submitted that their dependent claims which recite yet further distinguishing features of the invention are also patentable. These dependent claims need no further discussion herein.

**CONCLUSION**

In view of the amendments to the claims and the arguments provided herein, it is submitted that all the claims are patentable. Accordingly, a Notice of Allowance is requested in due course. If any extension and/or fee is required, authorization is given to charge Deposit Account No. 01-0484. Should any minor informalities need to be addressed, the Examiner is encouraged to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

**DRAFT**

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